In the claims:

1. (Original) An interface architecture in an integrated circuit comprising:

an FPGA portion of said integrated circuit having logic blocks for implementing logic functions and interconnect conductors for programmably connecting said logic blocks

an ASIC portion of said integrated circuit having mask programmed logic circuits and mask programmed interconnect conductors between said logic circuits; and

mask programmed dedicated interface tracks connected between said logic blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion.

2. (Original) The interface architecture of claim 1, wherein interconnect conductors in said FPGA portion include local routing resources.

3. (Original) The interface architecture of claim 1, further including interface buffers disposed in series with said dedicated interface tracks between said FPGA portion and said ASIC portion.

4. (Currently Amended) The interface architecture of claim 3 wherein each of said interface buffers includes:

an input buffer;

an output buffer, said output buffer connected to said input buffer;

three multiplexers ~~multiplexors~~, two of said multiplexers ~~multiplexors~~ connected to said output buffer and one of said multiplexers ~~multiplexors~~ connected to said input buffer; and

a configurable register, said configurable register connected to each of said multiplexers ~~multiplexors~~.

5. (Currently Amended) The interface architecture of claim 3 wherein each of said interface buffers includes:

an input buffer;

an output buffer, said output buffer connected to said input buffer;

three multiplexers ~~multiplexors~~, two of said multiplexers ~~multiplexors~~ connected to said output buffer and one of said multiplexers ~~multiplexors~~ connected to said input buffer; and

a memory store, said memory store connected to each of said multiplexers ~~multiplexors~~.

6. (Currently Amended) The interface architecture of claim 3 wherein each of said interface buffers includes:

an input buffer;

an output buffer, said output buffer connected to said input buffer;

three multiplexers ~~multiplexors~~, two of said multiplexers ~~multiplexors~~ connected to said output buffer and one of said multiplexers ~~multiplexors~~ connected to said input buffer; and

programmable elements, said programmable elements connected to each of said multiplexers ~~multiplexors~~.

7. (Original) The interface architecture of claim 1, further including an FPGA-ASIC routing channel arranged between said dedicated interface tracks and said ASIC portion.

8. (Original) The interface architecture of claim 7, wherein said FPGA-ASIC routing channel is mask-programmable.

9. (Original) The interface architecture of claim 7, wherein said FPGA-ASIC routing channel is field-programmable.

10. (Original) The interface architecture 1C of claim 1, further including JTAG buffers arranged between said dedicated interface tracks and said ASIC portion.

11. (Original) The interface architecture of claim 1, further including a plurality of I/O modules arranged on the perimeter of the IC.

12. (Original) The interface architecture of claim 11, wherein one or more of said I/O modules are connected to said FPGA portion through a routing channel.

13. (Original) The interface architecture of claim 11, wherein one or more of said I/O modules are connected to said ASIC portion.

14. (Original) The interface architecture of claim 9, further including a plurality of I/O modules arranged on the perimeter of the IC.

15. (Original) The interface architecture of claim 14, wherein one or more of said I/O modules are connected to said FPGA-ASIC routing channel.

16. (Original) The interface architecture of claim 1, wherein said ASIC portion is adjacent to one side of said FPGA portion.

17. (Original) The interface architecture of claim 1, wherein said ASIC portion is adjacent to two sides of said FPGA portion.

18. (Original) The interface architecture of claim 1, wherein said ASIC portion is adjacent to three sides of said FPGA portion.

19. (Original) The interface architecture of claim 1, wherein said ASIC portion is adjacent to four sides of said FPGA portion.

20. (Original) The interface architecture of claim 1, wherein said FPGA portion has a hierarchial design including a plurality of levels, each of said levels containing local routing resources and a plurality of blocks, each of said blocks including either a module or another of said levels.

21. (Original) An interface architecture in an integrated circuit comprising:

an FPGA portion of said integrated circuit having a plurality of levels, each of said levels containing local routing resources and a plurality of blocks, each of said blocks including either a module or another of said levels;

an ASIC portion of said integrated circuit having mask programmed interconnect conductors between logic portions of said ASIC portion;

mask programmed dedicated interface tracks connected between said modules or blocks in said FPGA portion and said mask programmed interconnect conductors in said ASIC portion.

22. (Original) The interface architecture of claim 21, wherein each of said blocks in said FPGA portion contains local routing resources.

23. (Original) The interface architecture of claim 21, further including interface buffers arranged between said dedicated interface tracks and said ASIC portion.

24. (Currently Amended) The interface architecture of claim 23 wherein each of said interface buffers includes:

an input buffer;

an output buffer, said output buffer connected to said input buffer;

three multiplexers ~~multiplexors~~, two of said multiplexers ~~multiplexors~~ connected to said output buffer and one of said multiplexers ~~multiplexors~~ connected to said input buffer; and

a configurable register, said configurable register connected to each of said multiplexers ~~multiplexors~~.

25. The interface architecture of claim 23 wherein each of said interface buffers includes:

an input buffer;

an output buffer, said output buffer connected to said input buffer;

three multiplexers ~~multiplexors~~, two of said multiplexers ~~multiplexors~~ connected to said output buffer and one of said multiplexers ~~multiplexors~~ connected to said input buffer; and

a memory store, said memory store connected to each of said multiplexers ~~multiplexors~~.

26. (Currently Amended) The interface architecture of claim 23 wherein each of said interface buffers includes:

an input buffer;

an output buffer, said output buffer connected to said input buffer;

three multiplexers ~~multiplexors~~, two of said multiplexers ~~multiplexors~~ connected to said output buffer and one of said multiplexers ~~multiplexors~~ connected to said input buffer; and

programmable elements, said programmable elements connected to each of said multiplexers ~~multiplexors~~.

27. (Original) The interface architecture of claim 21, further including an FPGA-ASIC routing channel arranged between said dedicated interface tracks and said ASIC portion.

28. (Original) The interface architecture of claim 27, wherein said FPGA-ASIC routing channel is mask-programmable.

29. (Original) The interface architecture of claim 27, wherein said FPGA-ASIC routing channel is field-programmable.

30. (Original) The interface architecture of claim 21, further including JTAG buffers arranged between said dedicated interface tracks and said ASIC portion.

31. (Original) The interface architecture of claim 21, further including a plurality of I/O modules arranged on the perimeter of the IC.

32. (Original) The interface architecture of claim 31, wherein one or more of said I/O modules are connected to said FPGA portion through a routing channel.

33. (Original) The interface architecture of claim 31, wherein one or more of said I/O modules are connected to said ASIC portion.

34. (Original) The interface architecture of claim 29, further including a plurality of I/O modules arranged on the perimeter of the integrated circuit.

35. (Original) The interface architecture of claim 34, wherein one or more of said I/O modules are connected to said FPGA-ASIC routing channel.

36. (Original) The interface architecture of claim 21, wherein said ASIC portion is adjacent to one side of said FPGA portion.

37. (Original) The interface architecture of claim 21, wherein said ASIC portion is adjacent to two sides of said FPGA portion.

38. (Original) The interface architecture of claim 21, wherein said ASIC portion is adjacent to three sides of said FPGA portion.

39. (Original) The interface architecture of claim 21, wherein said ASIC portion is adjacent to four sides of said FPGA portion.